



Digital VLSI Design with Verilog: A Textbook from Silicon Valley Technical Institute

By John Williams

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Digital VLSI Design with Verilog: A Textbook from Silicon Valley Technical Institute By John Williams

Verilog and its usage has come a long way since its original invention in the mid-80s by Phil Moorby. At the time the average design size was around ten thousand gates, and simulation to validate the design was its primary usage. But between then and now designs have increased dramatically in size, and automatic logic synthesis from RTL has become the standard design flow for most design.

Indeed, the language has evolved and been re-standardized too.

Over the years, many books have been written about Verilog. My own, coauthored with Phil Moorby, had the goal of defining the language and its usage, providing examples along the way. It has been updated with two new editions as the language and its usage evolved. However this new book takes a very different and unique view; that of the designer. John Michael Williams has a long history of working and teaching in the field of IC and ASIC design. He brings an in-depth presentation of Verilog and how to use it with logic synthesis tools; no other Verilog book has dealt with this topic as deeply as he has. If you need to learn Verilog and get up to speed quickly to use it for synthesis, this book is for you. It is sectioned around a set of lessons including presentation and explanation of new concepts and approaches to design, along with lab sessions.

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Editorial Review

From the Back Cover

This unique textbook is structured as a step-by-step course of study along the lines of a VLSI IC design project.

In a nominal schedule of 12 weeks, two days and about 10 hours per week, the entire verilog language is presented, from the basics to everything necessary for synthesis of an entire 70,000 transistor, full-duplex serializer - deserializer, including synthesizable PLLs.

Digital VLSI Design With Verilog is all an engineer needs for in-depth understanding of the verilog language: Syntax, synthesis semantics, simulation, and test. For a reader with access to appropriate electronic design tools, all solutions can be developed, simulated, and synthesized as described in the book.

A partial list of design topics includes design partitioning, hierarchy decomposition, safe coding styles, back-annotation, wrapper modules, concurrency, race conditions, assertion-based verification, clock synchronization, and design for test.

Coverage of specific devices includes basic discussion and exercises on flip-flops, latches, combinational logic, muxes, counters, shift-registers, decoders, state machines, memories (including parity and ECC), FIFOs, and PLLs. Verilog specify blocks, with their path delays and timing checks, also are covered.

Users Review

From reader reviews:

Judith Carter:

Have you spare time for any day? What do you do when you have much more or little spare time? That's why, you can choose the suitable activity for spend your time. Any person spent their very own spare time to take a go walking, shopping, or went to the particular Mall. How about open or even read a book titled Digital VLSI Design with Verilog: A Textbook from Silicon Valley Technical Institute? Maybe it is to get best activity for you. You recognize beside you can spend your time using your favorite's book, you can better than before. Do you agree with its opinion or you have some other opinion?

Naomi Taylor:

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Jerry Hull:

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Anthony Lainez:

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