



Digital Design and Modeling with VHDL and Synthesis (Systems)

By K. C. Chang

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Digital Systems Design with VHDL and Synthesis presents an integrated approach to digital design principles, processes, and implementations to help the reader design much more complex systems within a shorter design cycle. This is accomplished by introducing digital design concepts, VHDL coding, VHDL simulation, synthesis commands, and strategies together.

The author focuses on the ultimate product of the design cycle: the implementation of a digital design. VHDL coding, synthesis methodologies and verification techniques are presented as tools to support the final design implementation. Readers will understand how to apply and adapt techniques for VHDL coding, verification, and synthesis to various situations.

Digital Systems Design with VHDL and Synthesis is a result of K.C. Chang's practical experience in both design and as an instructor. Many of the design techniques and considerations illustrated throughout the chapters are examples of viable designs. His teaching experience leads to a step-by-step presentation that addresses common mistakes and hard-to-understand concepts in a way that eases learning.

Unique features of the book include the following:

- VHDL code explained line by line to capture the logic behind the design concepts
- VHDL is verified using VHDL test benches and simulation tools
- Simulation waveforms are shown and explained to verify design correctness
- VHDL code is synthesized and commands and strategies are discussed. Synthesized schematics and results are analyzed for area and timing
- Variations on the design techniques and common mistakes are addressed; Demonstrated standard cell, gate array, and FPGA three design processes
- Each with a complete design case study
- Test bench, post-layout verification, and test vector generation processes.

Practical design concepts and examples are presented with VHDL code, simulation waveforms, and synthesized schematics so that readers can better

understand their correspondence and relationships.

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Editorial Review

From the Back Cover

Combines VHDL and synthesis in an easy-to-follow step-by-step sequence. This approach addresses common mistakes and hard-to-understand concepts in a way that eases learning. Digital Design and Modeling with VHDL and Synthesis introduces VHDL with closely related practical design examples, simulation waveforms, and schematics so you can better understand their correspondence and relationship. This book is the result of the K.C. Chang's extensive experience in both design and teaching. Many of the design techniques and design considerations, illustrated throughout the chapters, are examples of real designs.

About the Author

K.C. Chang received his BS degree in Electrical Engineering from National Taiwan University in 1979. His MS and PhD degrees in computer science were earned at the University of Minnesota in 1984 and 1986. Later in 1986 he joined the Boeing Company where he teaches VHDL and synthesis courses in addition to his regular responsibilities of computer-aided design algorithm development, VHDL, synthesis and ASIC design. He has designed several ASICs with VHDL and synthesis including DSP and RISC 32-bit floating point microprocessors. He also gives conference tutorials on these same subjects. He earned his MBA degree at the City University in 1992. Dr. Chang holds 3 US patents. He has been an associate technical fellow at Boeing and an affiliate associate professor at the University of Washington Electrical Engineering Department since 1997.

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